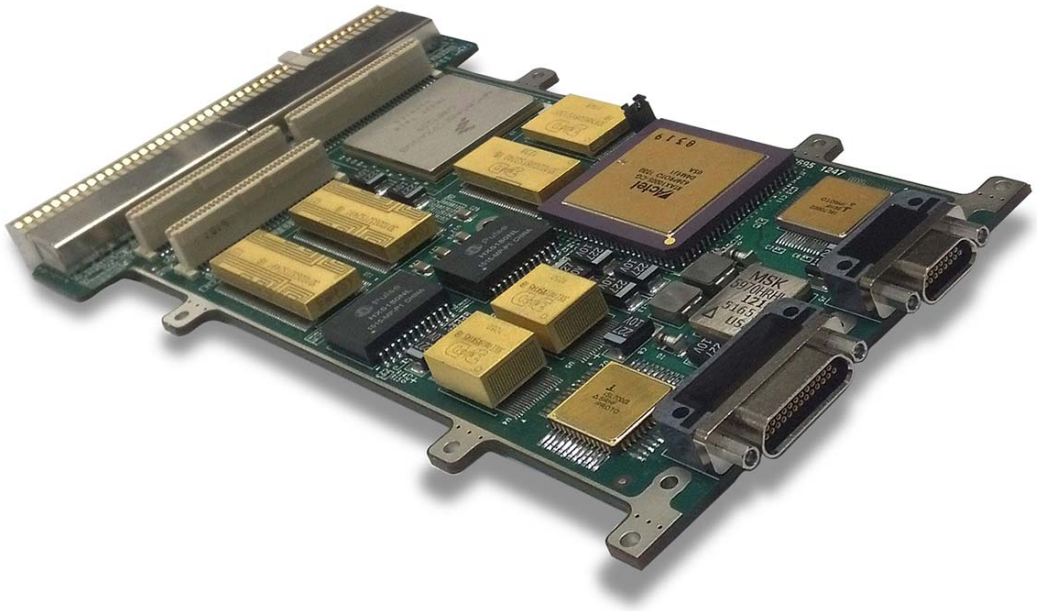
SP0
3U cPCI Radiation Tolerant PowerPC SBC



- *Rugged 3U CompactPCI SBC*
- *PowerQUICC-III MPC8548E @ 833 MHz, 1.0 and 1.17 GHz*
- *333 MHz Core Complex Bus (CCB) Speed*
- *One Standard PMC Site*
- *PICMG 2.0, Rev. 3.0 Compliant*
- *System Controller or Peripheral*
- *512MB of DDR1 SDRAM at 333 MHz with ECC*
- *Redundant 512KB Boot Memory*
- *1GB User Flash Memory (8GB Optional)*
- *Two 10/100/1000 Mbps Ethernet Ports*
- *Up to Four Async Serial RS-422 Ports*
- *Five Single Ended TTL I/O lines*
- *Four High Performance DMA Engines*
- *Four 32 bit Timers (Internal to the CPU)*
- *Three Watchdog Timers*
- *1PPS port for Timing Synchronization*
- *Three On-board Temperature Sensors (not available on Series 500 cards)*
- *Options for Front Panel Connectors*
- *VxWorks 6.x RTOS Support*
- *Available in Conduction Cooled Versions Series 100, 200 and 500*

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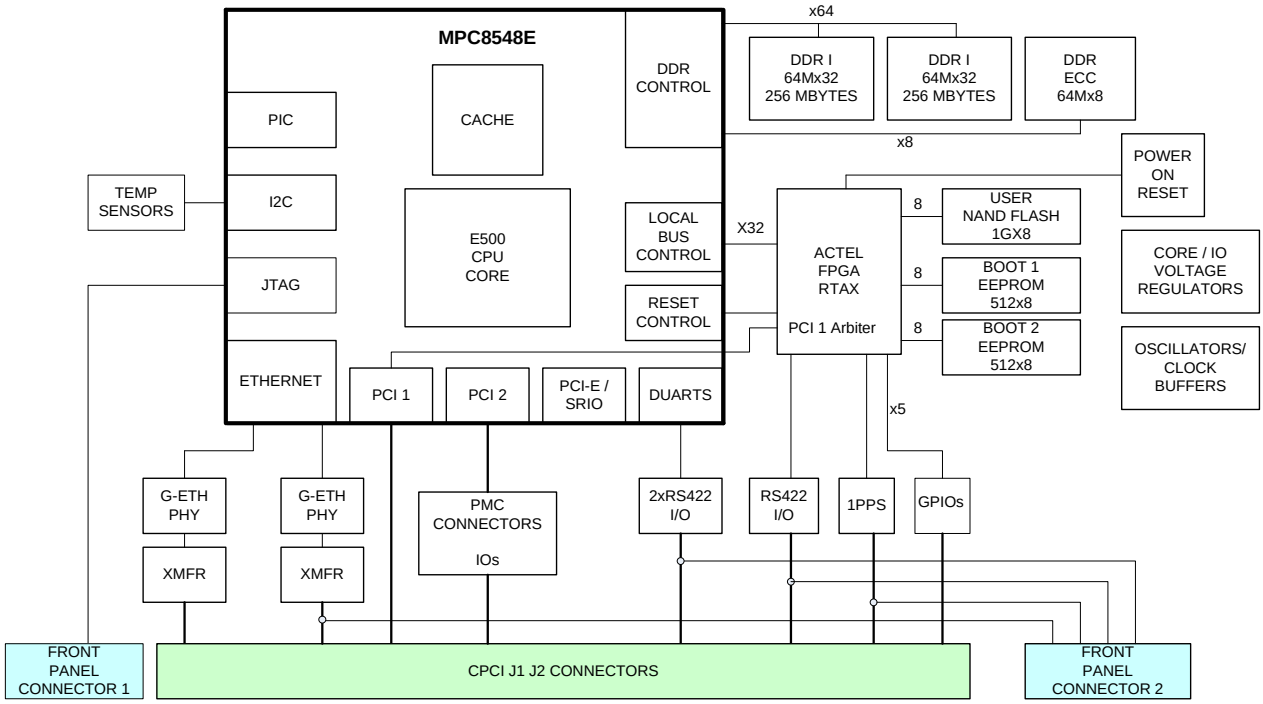
SP0 Powerful Processing for Space in Compact Form Factor

Aitech's SP0 3U CompactPCI SBC is an evolution from the Aitech C925/S950 SBCs. Modifications included a processor upgrade to the Freescale's PowerQUICC III MPC8548E – e500 System on Chip, an additional large user Flash. With the processor upgrade, the SP0 has increased processing performance while maintaining or reducing the power requirements.

The MPC8548E has an on-chip 32KB instruction and 32KB Data L1 caches as well as a 512KB L2 cache. The CPU speed can be configured to between 833 MHz and 1.166 GHz. And the CPU Core Complex Bus (CCB) is configured to 333 MHz.



For systems requiring maximum processing power, the SP0 processor can be configured to 1.17 GHz with CCB speed of 333.3 MHz.

The SP0 backplane connections were designed such that the SP0 can be configured as a one-to-one drop in replacement for the S950.

The SP0 implements large on-board memory size to support the processor and user application needs. Memory resources include 512MB 64 bits wide, fast DDR1 (Double Data Rate) SDRAM with ECC protection, from 1 to 8GB User Flash, 512KB redundant Boot EEPROM.

Onboard I/O capabilities of the SP0 include two (2) Gigabit Ethernet ports, four (4) high-speed serial communications ports and up to five (5) general-purpose discrete I/O channels. To further expand its capabilities, the SP0 is equipped with an industry standard conduction-cooled PMC slot allowing for installation of additional modules and functionality.

The SP0 may perform as either the CompactPCI system controller or as a peripheral board. When configured as system controller, the SP0 can support up to seven (7) additional cards on the CompactPCI backplane, providing clock, and arbitration and interrupt capabilities.

The highly integrated design of the SP0 guarantees performance and versatility for conduction- or air-cooled CompactPCI SBC aerospace applications.

Functional Description

Processor and System Architecture

The SP0 is a powerful processing platform achieved by combining a high performance PowerQUICC processor and extensive supporting memory arrays. In addition the board's architecture was designed to utilize all bus interfaces to the maximum.

Processor

The SP0 features Freescale's high performance MPC8548E PowerQUICC® 32-bit processor. Integrating both L1 (32 KB instruction/data) and L2 (512 KB) caches on chip supports its powerful e500 processing core.

The processor operates at from 833 MHz to 1.17 GHz with Core Complex Bus supporting running at 333 MHz speed.

It provides DDR1 controller bus and a scalable, flexible local bus to interface to memories such User Flash and Boot EEPROM.

The processor provides a large numbers of peripheral interfaces on-board such as dual serial ports, Ethernet ports, dual I^2C buses (Series 100 and 200 only), General Purpose I/Os, dual PCI buses.. These features reduce the number of peripheral cards needed to configure a fully functional subsystem.

Memory

The SP0 is equipped with large memory arrays. These arrays include 512MB fast DDR1 (Double Data Rate) SDRAM operating at 333 MHz, 1 to 8GB of User Flash memory (NAND Flash), and redundant 512 KB boot EEPROM. The DDR1 is connected directly to the processors DDR controller while the other memory resources reside on the processor's local bus through a FPGA.

The DDR1 SDRAM bank is ECC protected providing high data integrity. The DDR bus is 72 bit wide – 64-bit data and 8-bit ECC. It is hardware configured to operate at 333 MHz data rates.

CompactPCI Backplane

The SP0 utilizes one of the processor's PCI bus ports for the CompactPCI backplane interconnection, implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

In a CompactPCI subsystem, the SP0 is capable of performing either as a system controller, or as a peripheral card. As system controller, the SP0 supports up to seven additional cards on the PCI backplane providing them with clock signals and arbitration support.

Note: The SP0 cPCI interface supports only 3.3V signaling levels.

I/O Interfaces

In addition to its superior processing power, the SP0 provides many I/O capabilities (relative to its small form factor).

Secondary PCI Bus interface

The SP0 utilizes the second processor's PCI bus port for a PMC expansion site implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

PMC Expansion

The SP0 provides one IEEE 1386-2001 or ANSI/VITA 20-2001 compliant PMC expansion slot for extended flexibility and integration of additional I/O to the board.

The PMC is bus is 32 bit wide operating at 33 MHz.

The SP0 connects 24-48 dedicated PMC I/Os and optionally up-to 64 I/Os to the backplane.

Note: The PMC interface supports only 3.3 V signaling level.

Dual Ethernet Ports

Two (2) 10BaseT, 100BaseTX and 1000BaseT interfaces are provided on the SP0.

The Gigabit Ethernet controllers (MAC) are integrated in MPC8548E processor with internal FIFOs and DMA engines, allowing high bandwidth for data transfer through these interfaces. High performance physical layer devices complete this fast interface.

Serial Communication RS422 Ports

The SP0 provides three (3) asynchronous serial ports supporting RS422 physical interfaces. If 1PPS port is not used, it could be converted to the fourth RS422 serial port.

1PPS Port

There is a 1PPS input port for timing synchronization. It is on both front panel connector and backplane.

Discrete I/O

There are five discrete I/O channels routed to the CompactPCI backplane connectors.

I/O Routing

All 64 I/O interface signals are available at the SP0 J2 CompactPCI rear panel connectors. Select PMC I/O can be routed to the J2 connector trading off some of the on-board I/O functions and connectivity.

Front Panel Connectors

Many of the I/O interfaces are routed to the Front Panel Connectors. One for the processor JTAG and other for the RS422 interfaces, Ethernet interface and 1PPS interface.

System Support Devices

Watchdog Timers

The SP0 provides three watchdog timers. One is built in the MPC8548E processor which, when enabled, generates an internal CPU interrupt after the first internal timer expiration period and a hardware reset request after the second expiration period. The expiration period is programmable.

The second Watchdog timer is external to the processor. When enabled, it resets the whole board after the first expiration period.

The third watchdog timer is inside an on-board FPGA and is programmable. When enabled, it can reset the whole board or only certain IO devices after the expiration period.

Software

Test and Diagnostic Features

The SP0 is supplied with an extensive firmware package, including startup firmware (boot software), AIMon monitor/debugger tool, AIDiag diagnostic tool, and BIT. BIT may be executed during power-up or at any time after the board has been booted.

A JTAG/COP interface to the processor is provided for debugging and development purposes.

Operating Systems

The SP0 comes with complete Board Support Packages (BSP) for WindRiver VxWorks Version 6.7 and 6.9. (The BSP package can be optionally available for Green Hills Integrity and Linux upon request),

BSPs include drivers for all on-board resources, allowing the user to take full advantage of the SP0's powerful features.

Radiation Performance

Radiation Tolerant design with mitigation and/or immunity to SEE, TID and Latch-up. Radiation tested in UC Davis and IUCF to 100 krads(Si). The VxWorks BSP offers mitigation of Single Event Upsets; the resulting cross-sections are available upon request.

The MPC8548E processor is built in SOI technology and is immune to latch-up, other components in the standard configuration are latch-up immune to at least 37 MeV-cm2/mg. For detailed data on total dose and latch-up immunity please contact Aitech directly.

Component Selection

For Series 500, the flight-qualified parts used on the product are selected to meet or exceed Grade 2 NASA Goddard Space Flight Center (GSFC) EEE-INST-002, April 2008. Other component selection criteria are also available; please contact your Aitech representative for additional information.

Mechanical Features

The SP0 is available in conduction cooled per ANSI/VITA 30.1-2002 mechanical format. The mechanical format is a single slot 3U module with dimensions in accordance with the referenced specifications. For Series 200/500 level configurations that require a PMC, please refer to the User's Manual or contact Aitech for additional information.

A custom metal frame provides excellent rigidity, shock and vibration resistance. The frame also provides an array of stiffeners to support rugged PMC boards. The mass of 5SP0 is 0.77lb (350g).

Thermal Management

Careful mechanical design, including custom heatsink modules combined with a metal frame, allow for optimal heat dissipation and relief of the board. The SP0 is also equipped with three temperature sensors, located at temperature-critical locations, to monitor board temperature and provide temperature data to user application software. The sensors can be polled by the processor or send an alarm interrupt to the processor when they reach a certain temperature threshold. These thermal sensors are available on Series 100 and 200 only.

Power Requirements

The SP0 receives power from the CompactPCI backplane and generates its specific power supplies on-board. See ordering options table below.

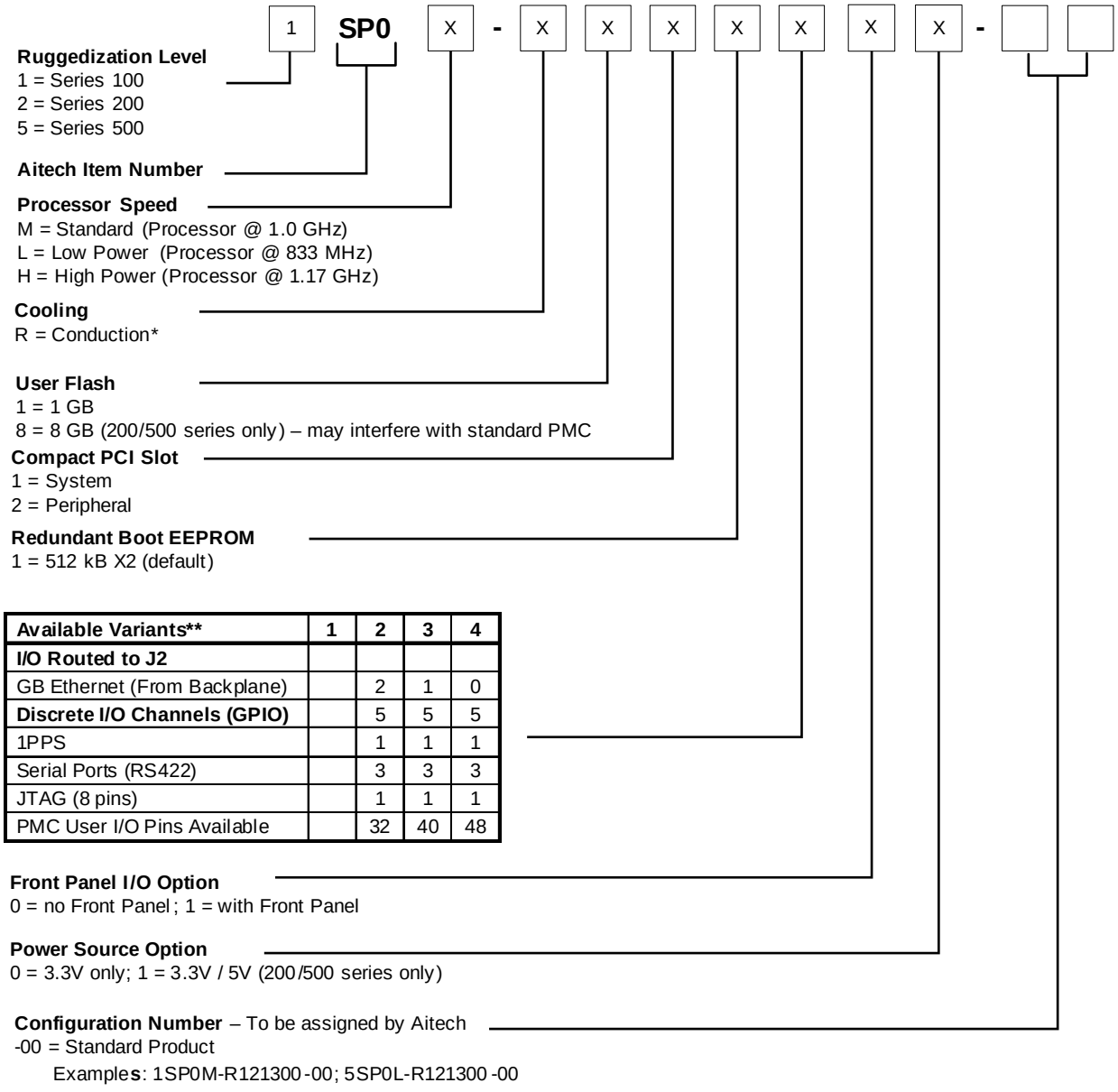
Power consumption for a fully populated SP0 with @833/333 MHz, 512MB SDRAM, 1GB Flash (no PMC installed):

	3.3V only		3.3V / 5V	
Supply	Typ.	Max	Typ.	Max
3.3Vdc	2.5 A	3.8 A	0.68 A	1.36 A
5Vdc	0 A	0 A	1.20 A	1.60 A
±12Vdc	0 A	0 A	0 A	0 A
Power	8.25 W	12.5 W	8.25 W	12.5 W

Environmental Features

Please Refer to the Aitech Ruggedization Datasheet.

Ordering Information for the SP0



Available Variants**	1	2	3	4
I/O Routed to J2				
GB Ethernet (From Backplane)		2	1	0
Discrete I/O Channels (GPIO)		5	5	5
1PPS		1	1	1
Serial Ports (RS422)		3	3	3
JTAG (8 pins)		1	1	1
PMC User I/O Pins Available		32	40	48

* - Series 100 Conduction cooled cards can be used in the air-cooled enclosures

** - Check with the factory if different I/O option is needed. Variant '1' is reserved.

Note: 5 Discrete I/O channels are pre-configured as 3 inputs (GPIO0…2) and 2 outputs (GPIO3 and GPIO4)

Aitech Defense Systems, Inc. **305-0014-01_7**

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