SP0-S

3U cPCI Radiation Tolerant PowerPC SBC

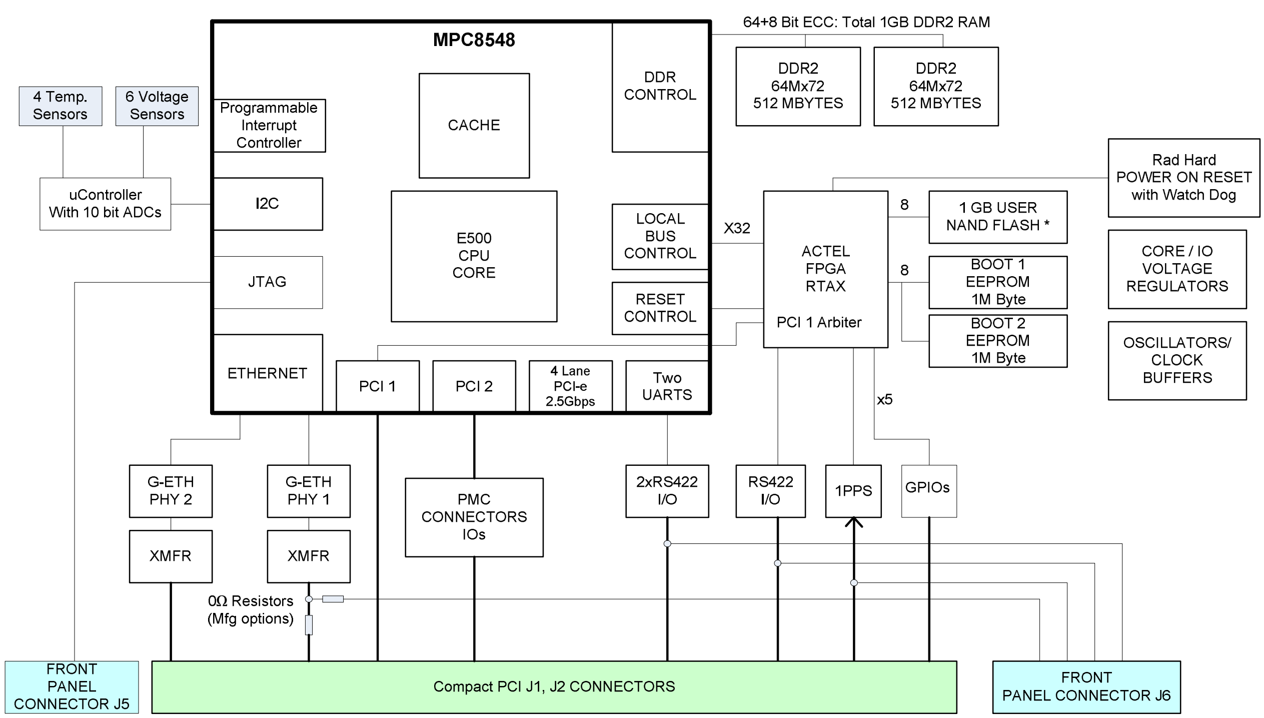
- ***Space-qualified, 3U CompactPCI SBC***
- ***PowerQUICC-III MPC8548E @ 1.0 GHz***
- ***400 MHz Core Complex Bus (CCB) Speed***
- ***One (1) Standard 32bit/33 MHz PMC Site***
- ***PICMG 2.0, Rev. 3.0 Compliant***
- ***System Controller or Peripheral***
- ***1GB of DDR2 at 400 MHz with ECC***
- ***1GB User Flash Memory[1] with ECC***
- ***Dual Redundant 1MB Boot Memory***
- ***One (1) or Two (2) Gb Ethernet Ports***
- ***Three (3) Async Serial RS-422 Ports***
- ***Five (5) Single Ended TTL I/O lines***
- ***Four (4) High Performance DMA Engines***
- ***Four (4) 32 bit Timers (Internal to the CPU)***
- ***Three (3) Watchdog Timers***
- ***1PPS port for Timing Synch.***
- ***Three (3) On-board Temperature Sensors***
- ***Six (6) on-board A/D voltage monitors***
- ***Options for Front Panel Connectors***
- ***VxWorks 6.x RTOS Support***
- ***Available in Conduction Cooled Versions Series 100, 200 and 500***
    - ***S500 utilize Hypertronics Hypertac cPCI backplane connectors***
- ***LEO, MEO and GEO Mission Options***

Aitech Defense Systems, Inc
A member of the Aitech Rugged Group
19756 Prairie St. Chatsworth, CA 91311
Tel: (888) Aitech-8 (248-3248) Fax: (818) 407-1502 e-mail: sales@rugged.com web: www.rugged.com

SP0-S Powerful Processing for Space in a Compact Form Factor

At the heart of Aitech's newly updated Space-rated SP0-S for LEO, MEO or GEO missions is NXP's (formally Freescale) PowerQUICC®III MPC8548E – e500 System on Chip. This further enhanced SP0-S 3U CompactPCI SBC represents an evolution from the previous generation of Space COTS SP0 SBC. Modifications include a performance enhancing, SDRAM memory upgrade to DDR2 doubling performance and increasing the Boot memory to 1MB for each redundant Flash. In addition, three, rad-hard, on-board temperature sensors and six (6) microcontroller-based A/Ds monitor the board's 3.3Vdc input voltage as well as five (5) internally generated CPU core and I/O voltages. With the DDR2 memory and recent processor upgrade, the SP0-S has increased processing performance while maintaining its low power dissipation.

500 Level SP0-S Block Diagram



The MPC8548E has an on-chip 32KB instruction and 32KB Data L1 caches as well as a 512KB L2 cache. Running at a CPU speed of 1GHz, the Core Complex Bus (CCB) is configured to 400 MHz.

The SP0-S backplane connections were designed such that the SP0-S can be configured as a one-to-one, drop-in backplane replacement for the previous generation SP0 and Aitech's popular IBM PPC 750-based S950.

The SP0-S implements large on-board memory to support the processor and user applications. Memory resources include 1GB of 64 bit-wide, fast DDR2 (Double Data Rate-2) SDRAM with ECC protection, 1GB of User Flash, and 1MB of redundant Boot EEPROM with failover protection.

Onboard I/O capabilities of the SP0-S include two (2) Gigabit Ethernet ports, three (3) high-speed serial communications ports (UARTs) and up to five (5) general-purpose discrete I/O channels. To further expand its capabilities, the SP0-S is equipped with an industry standard conduction-cooled PMC slot allowing for installation of additional modules and functionality.

The SP0-S can be factory configured to perform either as the CompactPCI system controller or as a peripheral board. When configured as system controller, the SP0-S can support up to seven (7) additional cards on the CompactPCI backplane providing clock, arbitration and interrupt servicing capabilities. The highly integrated design of the SP0-S guarantees performance and versatility for conduction- or air-cooled CompactPCI SBC aerospace applications.

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Functional Description

Processor and System Architecture

The SP0-S is a powerful processing platform achieved by combining a high performance PowerQUICC®III processor and extensive supporting memory arrays. In addition the board's architecture was designed to utilize all bus interfaces to the maximum.

Processor

The SP0-S features NXP's (formally Freescale) high performance MPC8548E PowerQUICC®III 2-bit processor. Integrating both L1 (32 KB instruction/data) and L2 (512 KB) caches on chip supports its powerful e500 processing core.

The processor operates at 1 GHz with a Core Complex Bus running at 400 MHz. The ACTEL FPGA augments the processor local bus by providing control of the redundant boot EEPROMs, interfaces to the User Flash and controls the various board reset functions.

The processor provides a large numbers of peripheral interfaces on-board such as dual serial ports, Ethernet ports, dual I^2C buses, General Purpose I/Os and dual PCI buses. These features reduce the number of peripheral cards needed to configure a fully functional subsystem.

Memory

The SP0-S is equipped with large memory arrays. These arrays include 1024MB fast DDR2 (Double Data Rate) SDRAM operating at 400 MHz, 1GB of User Flash memory (NAND Flash), and redundant 1024 KB boot EEPROM. The DDR2 is connected directly to the processors DDR controller while the other memory resources reside on the processor's local bus through a rad tolerant RTAX FPGA.

The DDR2 SDRAM bank is ECC protected providing high data integrity. The DDR bus is 72 bit wide – 64-bit data and 8-bit ECC. It is hardware configured to operate at 400 MHz data rates.

CompactPCI Backplane

The SP0-S utilizes one of the processor's PCI bus ports for the CompactPCI backplane interconnection, implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

The SP0-S is capable of performing either as a cPCI system controller, or as a peripheral card. As a system controller, the SP0-S supports up to seven additional cards on the PCI backplane providing them with clock signals and arbitration support.

Note: Series 500 Flight Units utilize the space-qualified Hypertronics Hypertac backplane connectors; these connectors are optional for Series 200. See Ordering Options and Notes below.

I/O Interfaces

In addition to its superior processing power, the SP0-S provides many I/O capabilities relative to its small form factor.

Secondary PCI Bus interface

The SP0-S utilizes the second processor's PCI bus port for a PMC expansion site implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

PMC Expansion

One (1) IEEE 1386-2001 or ANSI/VITA 20-2001 compliant PMC expansion slot for extended flexibility and integration of additional I/O to the board.

The PMC is bus is 32 bit wide operating at 33 MHz.

The SP0-S connects 24-48 dedicated PMC I/O pins and optionally up-to 64 I/Os to the backplane.

Note: The PMC interface supports only 3.3 V signaling levels.

Dual Ethernet Ports

One (1) or Two (2) 10BaseT, 100BaseTX and 1000BaseT interfaces are provided on the SP0-S (see Ordering Options and Notes below).

The Gigabit Ethernet controllers (MAC) are integrated in MPC8548E processor with internal FIFOs and DMA engines, allowing high bandwidth for data transfer through these interfaces. High performance physical layer devices complete this fast interface.

Serial Communication RS422 Ports

Three (3) asynchronous serial ports support RS422 physical interfaces. If 1PPS port is not used, this could be optionally converted to a fourth RS422 serial port (input only).

1PPS Port

There is a 1PPS input port for timing synchronization on both the front panel connector and the backplane.

Discrete I/O

There are five discrete I/O channels routed to the CompactPCI backplane connectors.

I/O Routing

All 64 I/O interface signals could be available at the SP0-S J2 CompactPCI rear panel connector. Select PMC I/O can be routed to the J2 connector trading off some of the on-board I/O functions and interface connectivity.

Front Panel Connectors

Select I/O interfaces are routed to the Front Panel Connectors, including: JTAG, RS422 serial ports, Ethernet interface and 1PPS interface.

System Support Devices

Watchdog Timers

The SP0-S provides three watchdog timers. One is internal to the MPC8548E processor which, when enabled, generates an internal CPU interrupt after the first internal timer expiration period and a hardware reset request after the second expiration period. The expiration period is programmable.

The second Watchdog timer is external to the processor. When enabled, it resets the whole board after the first expiration period.

The third watchdog timer is inside an on-board FPGA and is programmable. When enabled, it can reset the whole board, or only certain IO devices after the expiration period.

Software

Test and Diagnostic Features

The SP0-S is supplied with an extensive firmware package, including startup firmware (boot software), AIMon monitor/debugger tool, AIDiag diagnostic tool, and BIT. BIT may be executed during power-up or at any time after the board has been booted.

A JTAG/COP interface to the processor is provided for debugging and development purposes.

Operating Systems

A complete Board Support Package (BSP) for WindRiver VxWorks Version 6.7 and 6.9 is available. An optional BSP package for Green Hills Integrity, Linux or OAR RTEMS is available on request. BSPs include drivers for all on-board resources, allowing the user to take full advantage of the SP0's powerful features.

Radiation Performance

Radiation Tolerant design with mitigation and/or immunity to SEE, TID and Latch-up. Radiation tested in UC Davis and IUCF to 100 krads (Si) TID. The VxWorks BSP offers mitigation of Single Event Upsets; the resulting cross-sections are available upon request.

The MPC8548E processor is manufactured using 90nm SOI technology and is immune to latch-up; other components in the standard configuration are latch-up immune to at least 65 MeV-cm^2/mg for the SP0–S. Please contact your Aitech representative directly for the detailed data on total dose and latch-up immunity and related ordering options.

Component Selection

For Series 500, the flight-qualified parts used on the SP0-S product are selected to meet or exceed Grade 2 NASA Goddard Space Flight Center (GSFC) EEE-INST-002, April 2008. Other EEE component selection criteria (e.g. Grade 2 Enhanced with extended SEE immunity or Grade 3) are also available; please contact your Aitech representative for additional information.

Mechanical Features

The SP0-S is available in conduction-cooled per ANSI/VITA 30.1-2002 mechanical format. The mechanical format is a single slot 3U module with dimensions in accordance with the referenced specifications (see Mechanical ICD for deviations from the standard). For Series 200/500 level configurations that require a PMC, please refer to the User's Manual or contact Aitech for additional information. If the Front Panel Connectors are required for a 200/500 Series version then the heat sink will not fit the 3U standard at this end of the board and requires customization. Please contact Aitech for specific information. The metal frame provides excellent rigidity, shock and vibration resistance and provides an array of mechanical stiffeners to support rugged PMC boards. The mass of 5SP0-S is 0.77lb (350g).

Thermal Management

Careful mechanical design and customizable heatsink modules combined with a metal frame, allow for optimal heat dissipation of the board. The SP0-S is equipped with three temperature sensors, located at temperature-critical locations, monitor board temperature and providing thermal data to user application software. The sensors can be polled by the processor or send an alarm interrupt to the processor when they reach a certain temperature threshold. These thermal sensors are available on Series 100, 200 and 500 models.

Power Requirements

The SP0-S receives power from the CompactPCI backplane and generates its specific power supplies on-board. See ordering options table below. Power consumption for a fully populated SP0-S with @1000/400 MHz Core/CCB, 1GB SDRAM and 1GB (no PMC).

	3.3V only		3.3V I/O / 5V Core	
Supply	Typ.	Max	Typ.	Max
3.3Vdc	2.5 A	3.8 A	0.68 A	1.36 A
5Vdc	0 A	0 A	1.20 A	1.60 A
±12Vdc	0 A	0 A	0 A	0 A
Power	8.25 W	12.5 W	8.25 W	12.5 W

Environmental Features

Please Refer to the Aitech Ruggedization Datasheet.

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Aitech

EMCOMO

Germany:
EMCOMO Solutions AG
Industriestr. 10
89231 Neu-Ulm
Phone: +49 731 880351-0

aitech@emcomo.de
www.emcomo.de

Ordering Information for the SP0-S

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Ruggedization Level
1 = Series 100
2 = Series 200
5 = Series 500

Aitech Item Number

Configuration
1 = Standard SP0-S @ 1.0 GHz, DDR-2/ECC
2 = Enhanced SEE, Grade 2 parts @ 1.0 GHz, DDR-2/ECC
3 = EEE Grade 3 parts @ 1.0 GHz, DDR-2/ECC

Cooling
R = Conduction

User Flash
1 = 1GB
2 = 8GB

Compact PCI Slot
1 = System
2 = Peripheral

Redundant Boot EEPROM
1 = 512 KB X 2
2 = 1 MB X2 (default)

Available I/O Variants	1	2*	3	4	5
(I/O Routed to P2)	Resv.				
GB Ethernet (to/from backplane)	Resv.	2 (1)	1	0	0
Discrete I/O Channels (GPIO)**	Resv.	5	5	5	0
1 PPS Input (Typ. from GPS)	Resv.	1	1	1	0
Serial Ports (RS422)	Resv.	3	3	3	2
JTAG (8 pins)	Resv.	1	1	1	0
PMC User I/O Pins Available	Resv.	32	40	48	64

Front Panel I/O Option
0 = no Front Panel I/O; 1 = with Front Panel I/O

Power Source Option
0 = 3.3V (Standard); 1 = 5V CPU Core / 3.3V I/O (Series 200 / 500 options only)

Backplane Connectors Option
1 = Standard Press-fit cPCI connectors S100 & S200; 2 = Hypertronix Hypertac (S500, S200 optional)

Configuration Number – To be assigned by Aitech
- 00 = Standard Product

Examples : 1 SP0 S-R 121300-00 ; 5 SP0 S-R 121300-00

NOTES:
1. I/O variant 1 is reserved. Contact Aitech if different memory or I/O configuration options are required.
2. (*) Only one (1) GbE port is available for Series 500 SP0-S2, variant intended for enhanced GEO operation with high SEE immunity.
3. (**) Five (5) discrete I/O channels are pre-configured as 3 inputs (GPIO0…2) and 2 outputs (GPIO3 and GPIO4). Contact Aitech if different I/O configuration options are required.
4. Series 100 Conduction cooled cards can be used in either conduction cooled or lab-grade air-cooled enclosures using standard CompactPCI press-fit backplane connectors. Series 500 boards utilize the Hypertronics Hypertac soldered backplane connectors; optional on Series 200.

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